# University of California, Santa Barbara

Department of Electrical and Computer Engineering

ECE 152A – Digital Design Principles

Midterm Exam #1 - Solution

July 18, 2007

Name ______________________________________

Perm # ____________________________________

Lab Section ________________________________

| | | |
|---|---|---|
| Problem #1 | (20 points) | ____________ |
| Problem #2 | (20 points) | ____________ |
| Problem #3 | (20 points) | ____________ |
| Problem #4 | (20 points) | ____________ |
| Problem #5 | (20 points) | ____________ |
| Total | (100 points) | ____________ |

- This is a 75 minute exam; closed book, closed notes, no calculators.
- Answer all questions on the exam.

Problem #1.

For the Boolean expression given below:

$$A(B + C'D) + (BD)'C$$

a) (4 points) Using only Boolean algebra, give the equivalent expression in Sum of Products representation (you don't need to simplify the expression).

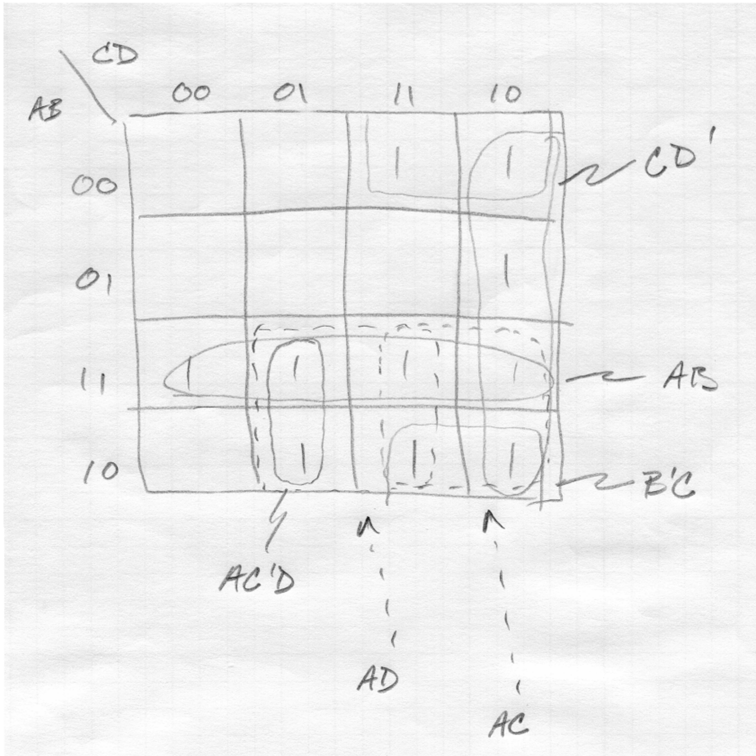
$$A(B+C'D) + (BD)'C$$

a) SUM OF PRODUCTS

$$A(B+C'D) + (B'+D')C$$

$$AB + AC'D + B'C + CD'$$

b) (4 points) Enter the function onto a Karnaugh map and identify the prime and essential prime implicants and find a minimal cover in Sum of Products form. Is the minimal cover unique?




PRIME IMPLICANTS:

AD, AC, B'C, AB, CD'

ESSENTIAL PRIME IMPLICANTS

AD, B'C, AB, CD'

MINIMAL COVER:

AD + B'C + AB + CD'

COVER IS UNIQUE BECAUSE IT INCLUDES ONLY ESSENTIAL, PRIME IMPLICANTS

c) (4 points) Using only Boolean algebra, give the equivalent expression in Product of Sums representation (begin with the minimized Sum of Products representation determined in part b above).

$$AB + AD + B'C + CD'$$

$$(A + AD)(B + AD) + (B' + CD')(C + CD')$$

$$A\,(A + B)(B + D) + (B' + C)(B' + D')\,C$$

$$A(B + D) + (B' + D')C$$

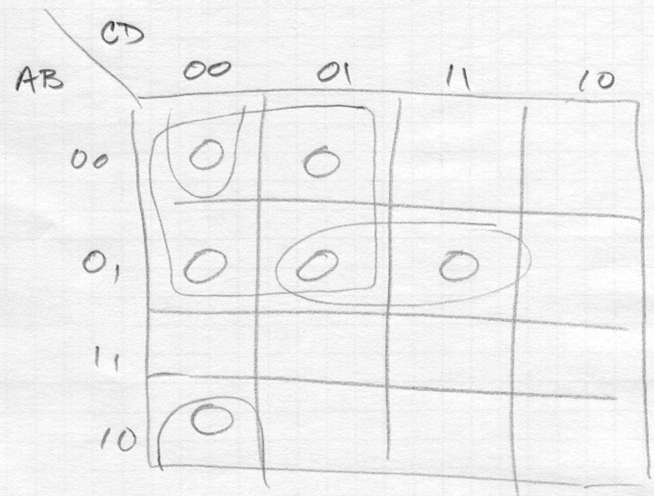
$$(A(B + D) + (B' + D'))(A(B + D) + C)$$

$$(AB + B' + AD + D')(A + C)(B + D + C)$$

$$(A + B' + A + D')(A + C)(B + D + C)$$

$$(A + B' + D')(A + C)(B + C + D)$$

d) (4 points) Again enter the function onto a Karnaugh map and identify the prime and essential prime implicants and a minimal cover in Product of Sums form. Is the minimal cover unique?




PRIME IMPLICANTS:

$(A+C)$, $(A+B'+D')$, $(B+C+D)$

ALL ARE ESSENTIAL, PRIME IMPLICANTS

MINIMAL COVER

$(A+C)(A+B'+D')(B+C+D)$

IS UNIQUE

e) (2 points) Express the function in canonical sum of minterms form (use the ∑m (...) notation.

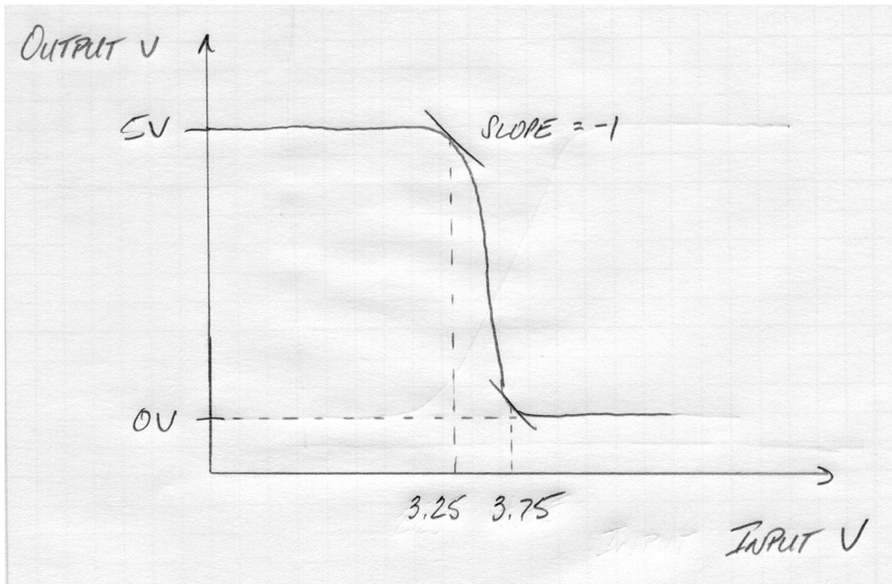
$$\sum m(2,3,6,9,10,11,12,13,14,15)$$

f) (2 points) Express the function in canonical product of Maxterms form (use the ∏ M (...) notation.

$$\prod M(0,1,4,5,7,8)$$

Problem #2.

a) The figure below illustrates the voltage transfer characteristic (V out vs. V in) for an inverter of unknown technology.




1. (4 points) What are the numeric values of VOH, VIH, VOL and VIL?

$V_{OH} = 5V$, $V_{OL} = 0V$

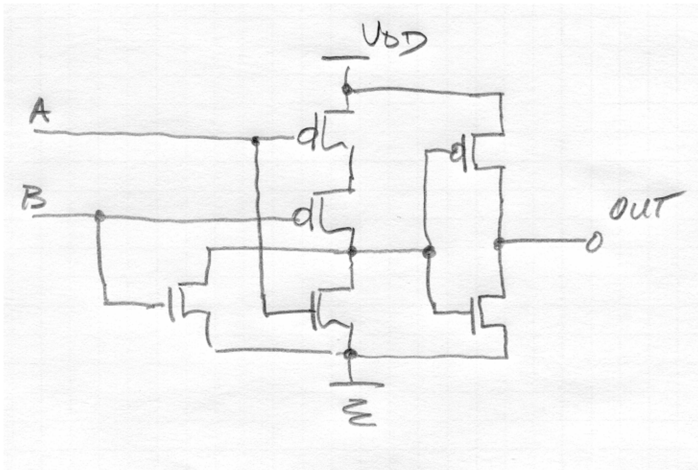
$V_{IH} = 3.75V$, $V_{IL} = 3.25V$

2. (4 points) What are the values of the high and low noise margins?

$NM_H = (5 - 3.75)V = 1.25V$

$NM_L = (3.25 - 0)V = 3.25V$

b) (4 points) What function is realized by the CMOS logic circuit shown below?

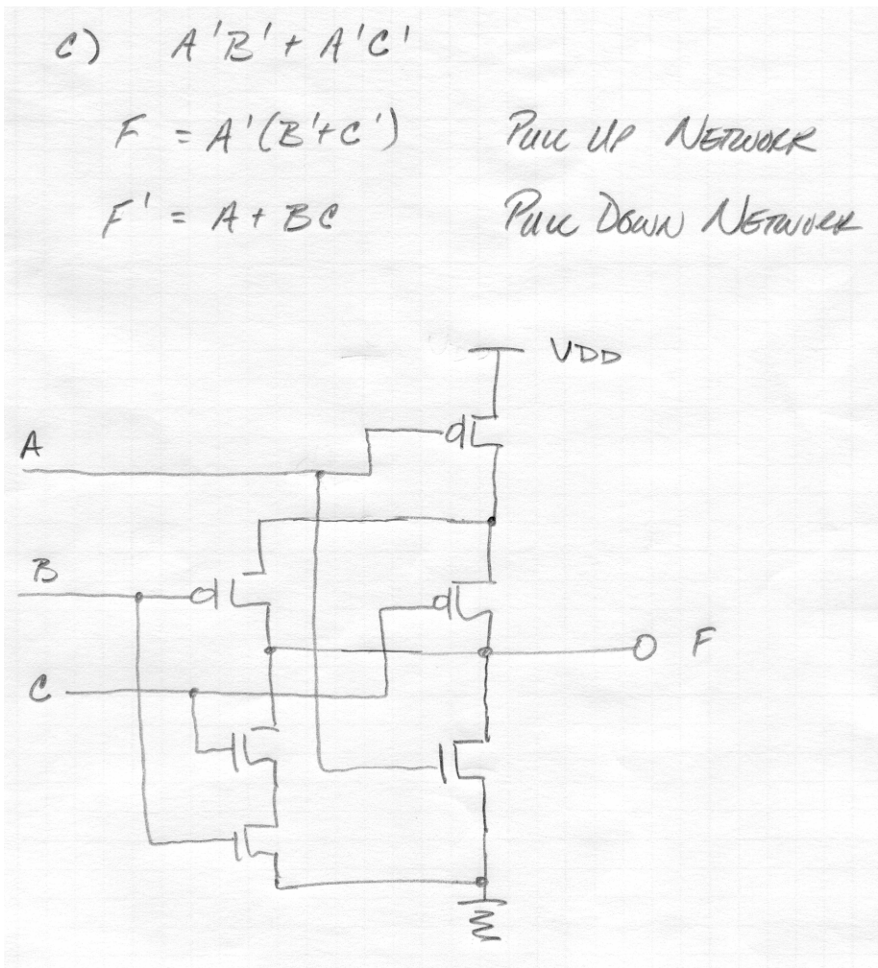



OUT = A + B (LOGICAL OR)

c) (8 points) Design the CMOS circuit (referred to as a “compound, static gate”) that realizes the function:

$$A'B' + A'C'$$

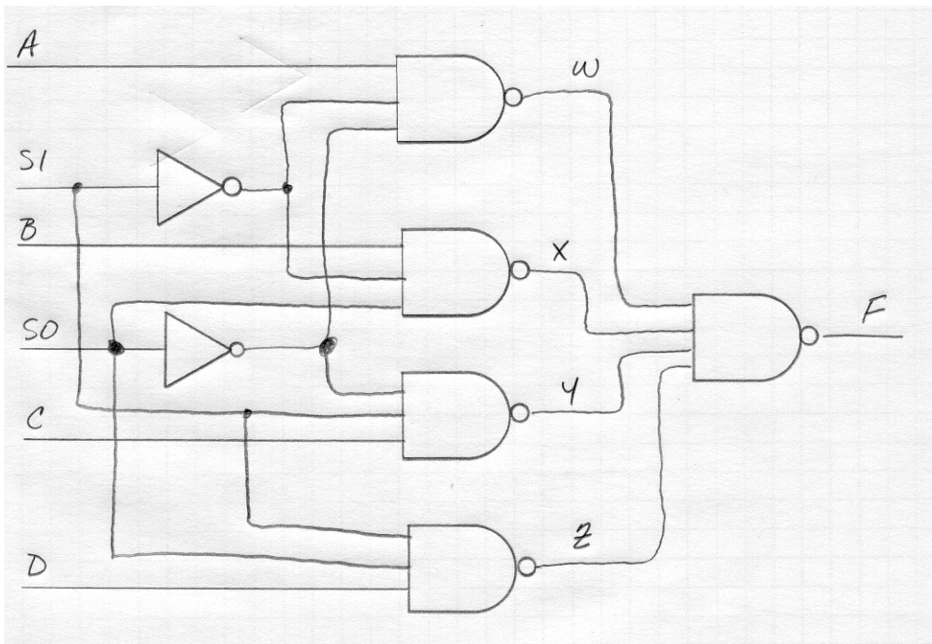
Your circuit should use the minimum number of transistors.



Problem #3.

a) (5 points) Identify the critical path and calculate the maximum propagation delay for the circuit shown below. The maximum propagation delays for the gates are:

| | tplh | tphl |
|---|---|---|
| Inverter | 15ns | 20ns |
| 3 input NAND | 17ns | 22ns |
| 4 input NAND | 20ns | 25ns |




CRITICAL PATH FROM S1 (OR S0) TO F

THREE LEVELS OF INVERSION

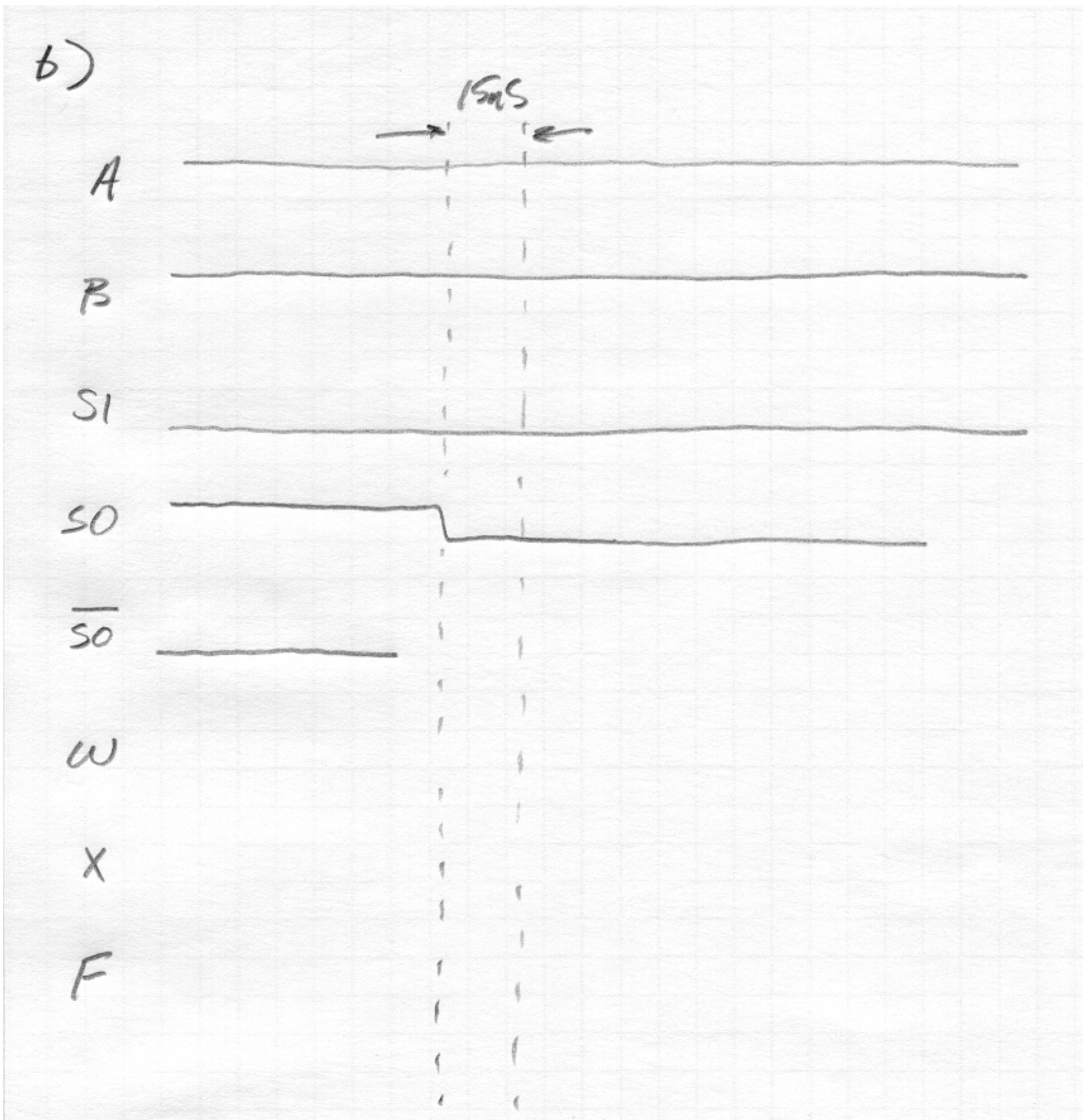
$t_{PLH} + t_{PHL} + t_{PLH} = 15 + 22 + 20 = 57nS$

OR

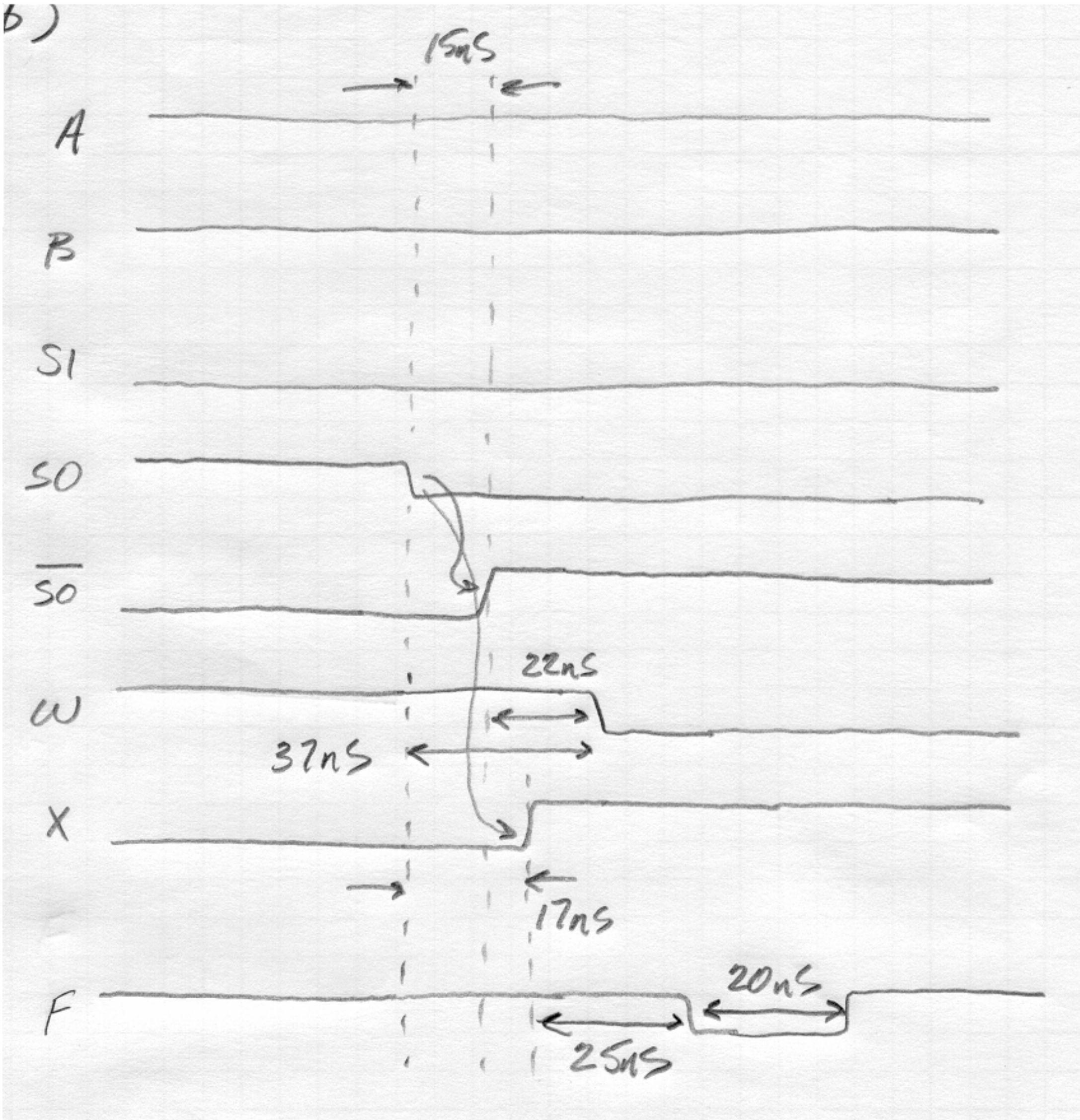
$t_{PHL} + t_{PLH} + t_{PHL} = 20 + 17 + 25 = \underline{62nS}$

↑ MAX PROP DELAY

b) (15 points) Using the maximum propagation delays from above, complete the timing diagram below. Initial conditions are A = 1, B = 1, S1 = 0 and S0 = 1. Indicate all delay times on the timing diagram.



b)



Problem #4.

a) (16 points) In this problem, you are asked to design the combinational circuit that examines the contents of a coin box and dispenses Coke® and change. The coin box accepts nickels and dimes and dispenses a Coke® when it detects 15¢ in the coin box and dispenses a Coke® and 5¢ change when it detects 20¢. Once the product and change have been delivered, the coin box is automatically emptied.

The circuit has four inputs, D1D0 (the binary representation of the number of dimes in the coin box) and N1N0 (the number of nickels). The circuit has two outputs K (Coke®) and C (change).

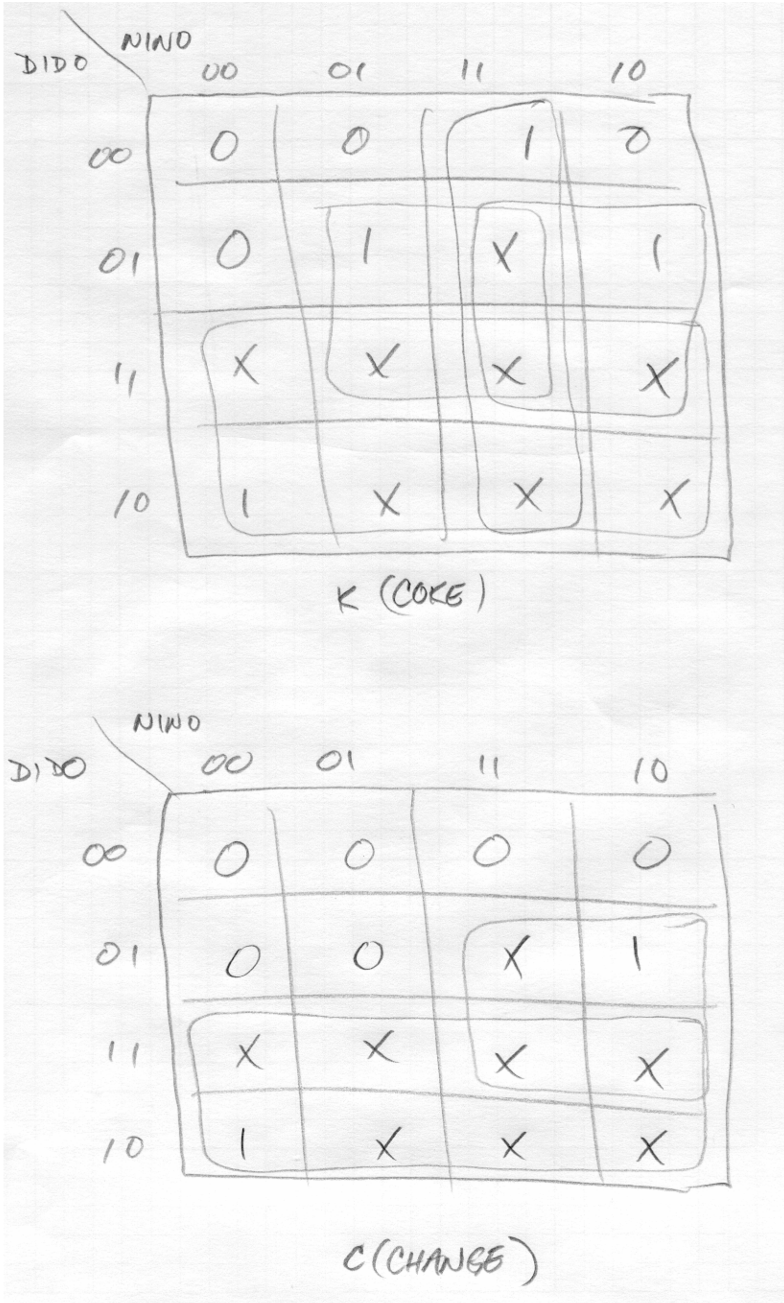
Design the circuit and implement it using only NAND gates. Assume you have the following TTL components available:

7400, quad, 2-input NAND gates
7406, hex inverters
7410, triple, 3-input NAND gates
7420, dual, 4-input NAND gates

Implement the circuit using the fewest number of IC's. Draw the schematic and indicate the components being used.

KEY OBSERVATION IS THAT THERE CAN NEVER BE MORE THAN 20¢ IN THE COIN BOX...
ANY INPUT > 20¢ IS A DON'T CARE

| D1 | D0 | N1 | N0 | K | C |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 | X | X |
| 1 | 0 | 0 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 | X | X |
| 1 | 0 | 1 | 0 | X | X |
| 1 | 0 | 1 | 1 | X | X |
| 1 | 1 | 0 | 0 | X | X |
| 1 | 1 | 0 | 1 | X | X |
| 1 | 1 | 1 | 0 | X | X |
| 1 | 1 | 1 | 1 | X | X |

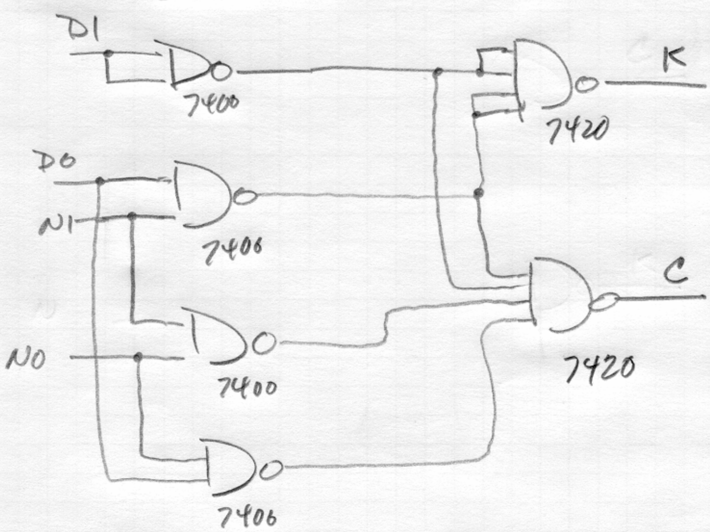

K (COKE)
C (CHANGE)

WITH NAND GATES:

$K = D1 + N1N0 + D0N0 + D0N1$

$C = D1 + D0N1$

NOTE: D1 AND D0N1 TERMS USED IN BOTH OUTPUTS




6 GATES, 2 IC's

1 7400, 1 7420

b) Marketing and sales has decided to raise the price of Coke® in its vending machines to 20¢ and to allow the machines to also accept quarters. Like the earlier version of the machine, any combination of nickels, dimes and quarters will result in delivery of the product and the appropriate change.

1) (2 points) How many inputs (bits) will this new circuit require (what determines the contents of the coin box)?

THERE NEED TO BE 6 INPUTS.
1 BIT – QUARTER
2 BITS – DIME
3 BITS – NICKEL (4 NICKELS NOW REQUIRED)

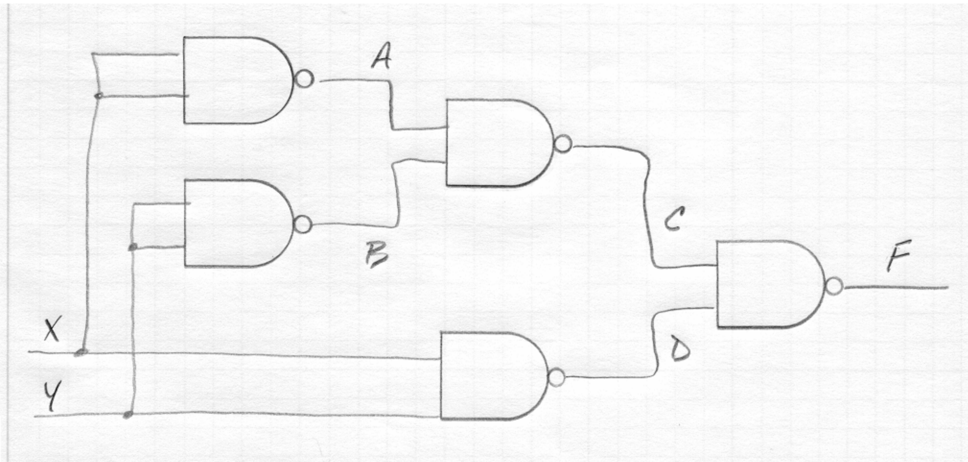
2) (2 points) How many different values of change (outputs) will this new circuit require?

THERE NEED TO BE 4 VALUES OF CHANGE:

5¢, 10¢, 15¢ AND 20¢

Problem #5.

For the logic circuit below:




a) (12 points) Give the structural (gate level) Verilog code that implements this circuit. Be sure to include all necessary declarations; the syntax doesn't have to be perfect, but all the elements must be present.

```
MODULE PROB_5 (F, X, Y);

  OUTPUT F;
  INPUT X, Y;
  WIRE X, Y, F, A, B, C, D;

  NAND (A, X, X);
  NAND (B, Y, Y);
  NAND (C, A, B);
  NAND (D, X, Y);
  NAND (F, C, D);

ENDMODULE
```

b) (8 points) Using Verilog's logical operators, rewrite the Verilog code (you don't have to repeat the declarations in this part).

USING THE LOGICAL OPERATORS

```
ASSIGN F = ~A & ~B | A & B;
```

OR

```
ASSIGN F = A ~^ B;
```